

**IN THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claim 1 (currently amended): A data reproduction device comprising a control circuit for reading out data recorded on a memory card having a controller mounted thereon, and a data processing circuit for giving required processing to the read data and outputting the generated data,

wherein the controller of the memory card is so constructed that an active mode is set for reading out the data with a current consumption of a first current value in response to memory access of data reading and thereafter automatically follows to a standby mode for waiting for next memory access with a non-zero current consumption of a second current value less than the first current value,

wherein the control circuit comprises a buffer for temporarily storing the data to be read out from the memory card, first control means to read out the data from the memory card at a first bit rate of 8 Mbps to store the generated data to the buffer, and second control means to read out the data stored in the buffer at a second bit rate ~~less than the first bit rate~~ of 128 Kbps to supply the read data to the data processing circuit, and while the data is intermittently read out from the memory card and stored in the buffer according to the first control means, the data is read out from the buffer according to the second control means.

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Claim 2 (original) A data reproduction device according to claim 1 wherein the first control means starts reading new data when predetermined space capacity is generated in the buffer by the second control means reading out the data from the buffer.

Claim 3 (original) A data reproduction device according to claim 1 wherein the controller of the memory card is so constructed that the standby mode follows when there is no memory access within a predetermined period of time after setting the active mode.

Claim 4 (original) A data reproduction device according to claim 1 wherein the control circuit repeats the intermittent read-out using the buffer until all the data to be reproduced is read out from the memory card.